Copyright WILEY-VCH Verlag GmbH & Co. KGaA, 69469 Weinheim, Germany, 2015.

ADVANCED MATERIALS

Supporting Information

for *Adv. Mater.,* DOI: 10.1002/adma.201405511

15.7% Efficient 10-μm-Thick Crystalline Silicon Solar Cells Using Periodic Nanostructures

*Matthew S. Branham, Wei-Chun Hsu, Selcuk Yerci, James Loomis, Svetlana V. Boriskina, Brittany R. Hoard, Sang Eon Han, and Gang Chen**

Copyright WILEY-VCH Verlag GmbH & Co. KGaA, 69469 Weinheim, Germany, 2013.

Supporting Information

15.7% Efficient 10-μm-Thick Crytalline Silicon Solar Cells Using Periodic Nanostructures

*Matthew S. Branham, Wei-Chun Hsu, Selcuk Yerci, James Loomis, Svetlana V. Boriskina, Brittany R. Hoard, Sang Eon Han, Gang Chen**

DETAILS ON THE CALCULATION OF FIGURE 3

Figure 3 is plotted in 10 nm increments. For a given wavelength increment, the "converted" photons were found by measuring the device EQE with an illuminated area that spanned several of the top contacts, such that reflection from the top contacts is incorporated into the quantum efficiency measurement. (Note that this is only for the purposes of Fig. 3. Quantum efficiency represented elsewhere in the article is for the absorber only.) "Top contact reflection" is taken as 2.2% (the areal fraction of metal coverage) of the incident photons at a given wavelength. "All other reflection" losses are found by subtracting "top contact reflection" from the total reflection, which was also measured with a light spot that spanned several contact lines. "Top nitride parasitic absorption" is calculated by multiplying the nitride absorptance (from COMSOL optical simulation) with the measured total absorption of the device. Similarly, the "back contact parasitic absorption" and "back reflector parasitic absorption" losses are calculated by multiplying the absorptance data from separate simulations (for bare aluminum and for oxide-cladded alumninum respectively) by the measured total absorption of the device, as well as by the approximate fraction of the back surface represented by each situation (8.7% and 91.3%, respectively). The approximate contribution of the two remaining loss mechanisms, recombination in the emitter and top surface and recombination in the bulk and back surface, are calculated by subtracting the "converted (measured)" and three sources of parasitic absorption loss from the total measured

absorbed photons and multiplying this amount by the fraction of photons absorbed in the emitter ("front surface and Auger recombination") and in the base using ("rear surface and bulk recombination") using the results of COMSOL optical simulation.

DEVICE FABRICATION

Surface pattern fabrication: An SOI wafer (Vendor: Ultrasil; device layer: 10 µm thick, p-type, ρ=0.6-0.85 Ω-cm; buried oxide layer: 250 nm thick; handle layer: 500 µm thick, p-type, ρ=1-5 Ω-cm) was first RCA cleaned, coated with 50 nm LPCVD nitride, and patterned with a two-dimensional array of holes on a 700nm pitch using projection lithography. The nitride film was etched using an SF_6/O_2 RIE chemistry, which subsequently served as a hard mask for a potassium hydroxide (KOH) anisotropic silicon etch to form the inverted pyramid surface texturing. The remaining nitride was dissolved in hot phosphoric acid (165°C). *Mesa die definition*: A virgin LPCVD film was deposited on the wafer and patterned using a contact aligner. The nitride was again etched using a CF_4/O_2 RIE chemistry, and the silicon surrounding the device dies etched away in KOH to leave sixteen 1 cm^2 silicon mesas/dies with sloped sidewalls, ensuring complete electrical isolation and precise area definition of the solar cells. The nitride was stripped in hot phosphoric acid at 165°C. *Selective top contact formation*: A 100 nm PECVD oxide film was deposited on the top surface and patterned with seven 30 µm wide stripes spanning the width of each die that were subsequently etched in 7:1 buffered oxide etch (BOE) to reveal the underlying silicon. Before sending the devices out for ion implantation, a dry thermal oxide was grown at 1000°C for 20 minutes, yielding a total oxide thickness of 30 nm (on (100) surfaces) in the contact regions and 100 nm everywhere else on the die. Selective n-type contacts were formed by two-step ion implantation: an initial low dose, high energy implant to dope the n-type top emitter (Phophorus, 110 keV, 9e14 cm^{-2}, 7° tilt) followed by a low energy, high dose implant to form the n^+ top contact regions (Arsenic, 70 keV, 2.8e15 cm^{-2}, 7° tilt). The implanted wafers were cleaned twice in

piranha, then cleaned again in RCA before diffusing at 1000°C for 60 minutes The target junction depth in the non-contact regions was ~600nm (on a planar surface) with a peak doping of 2.1 x 10^{19} cm^{-3}, while the peak doping in the contact region was designed to be 1.4 x 10^{20} cm^{-3}. The sheet resistance of the non-contact regions of the emitter was measured to be 60-80 Ω/☐ after annealing. *ARC Deposition*: The heavily-damaged implant oxide was stripped in BOE, and a high-quality, 100 nm-thick PECVD anti-reflection coating was deposited at T = 400°C using silane, ammonia, and nitrogen as precursor gases. *Top contact via fabrication*: Ten-micrometer-wide contact vias were lithographically aligned to the heavily-doped regions of the emitter followed by magnetically-enhanced reactive ion etching (MERIE) of the silicon nitride ARC in a CF_4/O_2 chemistry. *Rear window definition*: The rear windows were defined lithographically using back-side alignment, each slightly larger than 1 cm^2, followed by dry etching of the underlying LPCVD silicon nitride using an SF_6/O_2 chemistry. *Top contact formation*: The top metal contacts were formed using by patterning resist on the top-side of the wafer, followed by e-beam deposition of a 40 nm titanium adhesion layer, 40 nm palladium transition layer, and 920 nm silver conduction layer, and finally lifting off the undesired metal in acetone. The contacts were designed such that only the seven 30-µm-wide contact fingers, aligned to the top contact vias, traversed the device. The fingers continued down the KOH-etched sidewalls of the device before reaching the busbars, which were located over the handle of the SOI to allow probing without damaging the thin membrane. *Membrane etch*: The top circuitry and nitride ARC were protected by spinning a double coating of Pro-TEK B3 (Brewer Science), which after baking cures into an alkaline-resistant polymer film. Membrane release was accomplished by etching in a 20% KOH solution at 80°C for 7 hours and using the buried oxide as an etch stop. *Back contact formation and annealing*: After removing the Pro-TEK film in acetone, photoresist was dispensed into the backside window well of each die and thinned by spinning before patterning with ~25 µm diameter holes using a contact aligner, followed by etching of the

buried oxide layer using 7:1 buffered oxide etch (BOE) to produce contact openings to the backside silicon. A 600nm aluminum film was sputtered over the backside of the device wafer for back contact. Finally, the device was annealed in forming gas (14:1 N_2:H_2) at 475°C for ten minutes.

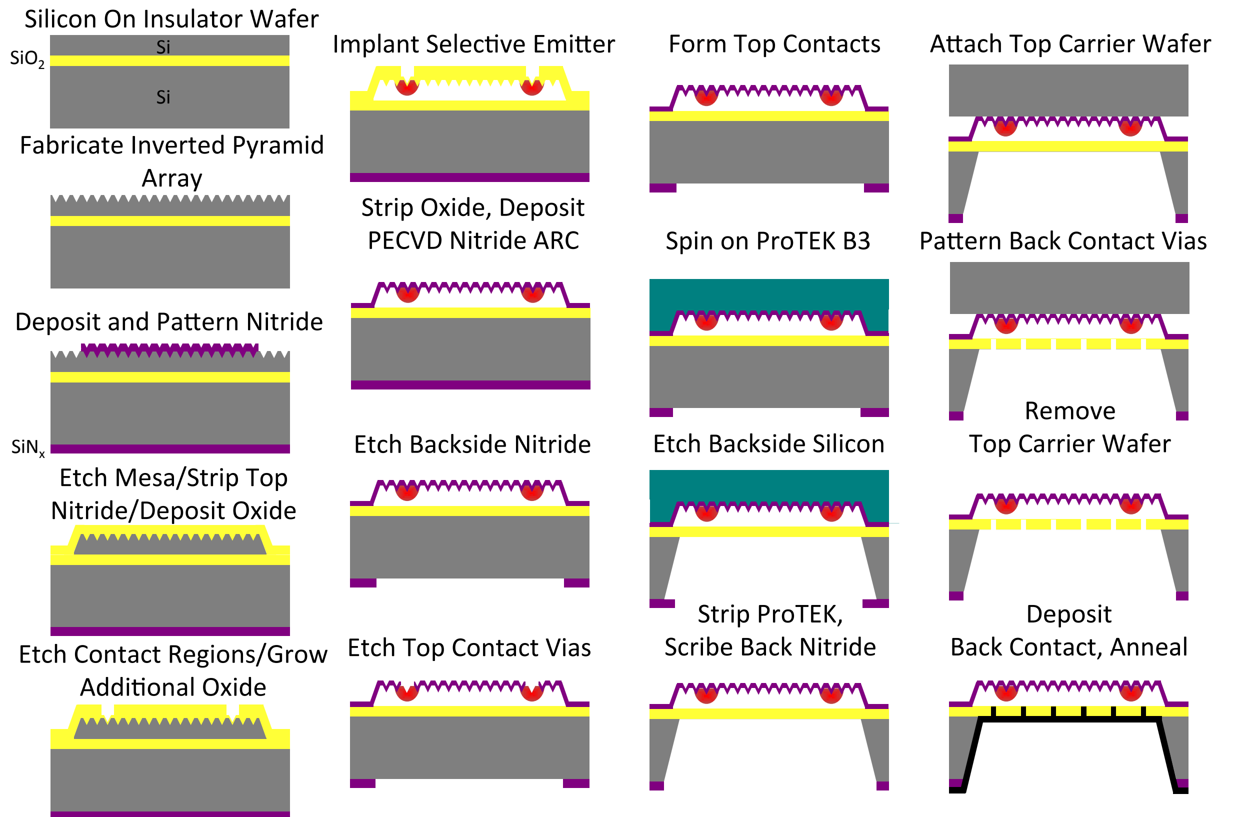

Figure S1: Ultrathin crystalline silicon solar cell with integrated photonic crystal fabrication process flow schematic

ACKNOWLEDGEMENTS ADDENDUM

Disclaimer: The information, data, or work presented herein was funded in part by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily

constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.